UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/840,173	05/05/2004	Koji Hamaguchi	259052004500	7492

25226 7590 08/11/2005

MORRISON & FOERSTER LLP
755 PAGE MILL RD
PALO ALTO, CA 94304-1018

EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/840,173	HAMAGUCHI ET AL.	
	Examiner	Art Unit	
	Thomas L. Dickey .	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/5/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 05/05/04 is acceptable.

Drawings

2. The formal drawings filed on 05/05/04 are acceptable.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

4. The Information Disclosure Statement filed on 05/05/04 has been considered.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225

USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

A. Claims 8-13 and 19-23 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-6 and 8 of copending Application No. 10/846875 in view of LARSEN ET AL. (5,537,350).

(1) With regard to claims 8-13, Claims 1-6 and 8 of said copending application disclose a memory structure with (i) a side-wall memory array including a plurality of side-wall memory transistors and sets of bitlines, each side-wall memory transistor having a side-wall portion; (iii) a plurality of switching circuits for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array; and (iv) logic circuitry for enabling the plurality of switching circuits in a selected sequential order, wherein each of the side-wall memory transistors comprises: a gate electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer;

a channel region formed below the gate electrode; a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units formed on the both sides of the gate electrode and having a function of retaining charges, and wherein the side-wall memory transistors are in sets and wherein selected switching circuit of the plurality of switching circuits is connected to a selected set of the sets of bitlines, and said selected switching circuit of the plurality of switching circuits is enabled to transfer a first voltage to the selected set of the sets of bitlines, the selected set being coupled to a set of the sets of side-wall memory transistors to be programmed, until the set of side-wall memory transistors to be programmed has been programmed and the logic circuitry comprises a state machine, the state machine enabling each of the plurality of switching circuits such that the voltage is applied individually to the sets of bitlines until each set of the sets of bitlines has been programmed, and a bit line select circuit coupled to the switching circuit to select bitlines of a set to connect to receive the voltage such that the selected bitlines are programmed. Claims 1-6 and 8 of said copending application do not disclose a charge pump for providing a voltage to accumulate negative charges in each memory transistor during a programming operation, or that the plurality of switching circuits comprise four switching circuits, each switching circuit coupled to a corresponding set of four bitlines.

However, Larsen et al. discloses a memory structure with a charge pump 30 for providing a voltage to accumulate negative charges in memory transistors during a

programming operation and a plurality switching circuits 44,45,46, and 47 for transferring the voltage to selected sets of a sets of bitlines of a memory array comprising four (44,45,46, and 47) switching circuits coupled to a corresponding set of four bitlines (seen without part # in figure 4, note column 8 line 11). Note figures 2-4, column 7 lines 7-40, and column 8 lines 4-17 of Larsen et al. Therefore, it would have been obvious to a person having skill in the art to augment claims 1-6 and 8 of said copending application's memory structure with the charge pump for providing a voltage to accumulate negative charges in each memory transistor during a programming operation and the plurality of switching circuits comprising four switching circuits coupled to a corresponding set of four bitlines such as taught by Larsen et al. in order to reduce the amount of current used in programming flash EEPROM memory arrays to thus provide a programmable EEPROM array with a more reasonable current requirement, or else to program a larger EEPROM array with the same current source.

(2) With regard to claims 19-23, claims 1-6 and 8 of said copending application disclose a structure for providing storage of data with (i) a side-wall memory array including a plurality of side-wall memory transistors and sets of bitlines, each side-wall memory transistor having a side-wall portion; (iii) a plurality of transferring means (switching circuits) for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array; and (iv) enabling means (logic circuitry) for enabling the plurality of transferring means (switching circuits) in a selected sequential order, wherein each of the side-wall memory transistors comprises: a gate electrode formed

on a semiconductor layer with a gate insulating film formed on the semiconductor layer; a channel region formed below the gate electrode; a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units formed on the both sides of the gate electrode and having a function of retaining charges, and wherein the side-wall memory transistors are in sets and wherein selected transferring means (switching circuit) of the plurality of transferring means (switching circuits) is connected to a selected set of the sets of bitlines, and said selected transferring means (switching circuit) of the plurality of transferring means (switching circuits) is enabled to transfer a first voltage to the selected set of the sets of bitlines, the selected set being coupled to a set of the sets of side-wall memory transistors to be programmed, until the set of side-wall memory transistors to be programmed has been programmed and the enabling means (logic circuitry) comprises a state machine, the state machine enabling each of the plurality of transferring means (switching circuits) such that the voltage is applied individually to the sets of bitlines until each set of the sets of bitlines has been programmed. Claims 1-6 and 8 of said copending application do not disclose a charge pump for providing a voltage to accumulate negative charges in each memory transistor during a programming operation, or that the plurality of means for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array comprise four switching circuits, a switching circuit is coupled to a corresponding set of four bitlines.

However, Larsen et al. discloses a structure for providing storage of data with a charge pump 30 for providing a voltage to accumulate negative charges in memory transistors during a programming operation and a plurality of means (switching circuits 44,45,46, and 47) for transferring the voltage to selected sets of a sets of bitlines of a memory array comprising four (44,45,46, and 47) switching circuits coupled to a corresponding set of four bitlines (seen without part # in figure 4, note column 8 line 11). Note figures 2-4, column 7 lines 7-40, and column 8 lines 4-17 of Larsen et al. Therefore, it would have been obvious to a person having skill in the art to augment claims 1-6 and 8 of said copending application's structure for providing storage of data with the charge pump for providing a voltage to accumulate negative charges in each memory transistor during a programming operation and a plurality of means for transferring the voltage to selected sets of a sets of bitlines of a memory array comprising four switching circuits coupled to a corresponding set of four bitlines such as taught by Larsen et al. in order to reduce the amount of current used in programming flash EEPROM memory arrays to thus provide a programmable EEPROM array with more reasonable current requirement, or else to program a larger EEPROM array with the same current source.

B. Claims 1-7 and 14-18 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 10,11 and 13-15 of copending Application No. 10/846875 in view of LARSEN ET AL. (5,537,350).

(1) With regard to claims 1-7, claims 10,11, and 13-15 of said copending application disclose a computer system with (A) a CPU; (B) a structure for providing storage of data comprising (i) a side-wall memory array including a plurality of side-wall memory transistors and sets of bitlines, each side-wall memory transistor having a side-wall portion; (iii) a plurality of switching circuits for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array; and (iv) logic circuitry for enabling the plurality of switching circuits in a selected sequential order, wherein each of the side-wall memory transistors comprises: a gate electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer; a channel region formed below the gate electrode; a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units formed on the both sides of the gate electrode and having a function of retaining charges, and wherein the side-wall memory transistors are in sets and wherein selected switching circuit of the plurality of switching circuits is connected to a selected set of the sets of bitlines, and said selected switching circuit of the plurality of switching circuits is enabled to transfer a first voltage to the selected set of the sets of bitlines, the selected set being coupled to a set of the sets of side-wall memory transistors to be programmed, until the set of side-wall memory transistors to be programmed has been programmed and the logic circuitry comprises a state machine, the state machine enabling each of the plurality of switching circuits such that the voltage is applied individually to the sets of bitlines until each set of the sets of

bitlines has been programmed, and (C) a system bus means for transferring data and addresses between the CPU and the structure for providing storage of data. Claims 10,11, and 13-15 of said copending application do not disclose a charge pump for providing a voltage to accumulate negative charges in each memory transistor during a programming operation, or that the plurality of switching circuits comprise four switching circuits, each switching circuit coupled to a corresponding set of four bitlines; and a bit line select circuit coupled to the switching circuit to select bitlines of a set to connect to receive the voltage such that the selected bitlines are programmed.

However, Larsen et al. discloses a computer system with a charge pump 30 for providing a voltage to accumulate negative charges in memory transistors during a programming operation and a plurality switching circuits 44,45,46, and 47 for transferring the voltage to selected sets of a sets of bitlines of a memory array comprising four (44,45,46, and 47) switching circuits coupled to a corresponding set of four bitlines (seen without part # in figure 4, note column 8 line 11). Note figures 2-4, column 7 lines 7-40, and column 8 lines 4-17 of Larsen et al. Therefore, it would have been obvious to a person having skill in the art to augment claims 1-6 and 8 of said copending application's computer system with the charge pump for providing a voltage to accumulate negative charges in each memory transistor during a programming operation and the plurality of switching circuits comprising four switching circuits coupled to a corresponding set of four bitlines such as taught by Larsen et al. in order to reduce the amount of current used in programming flash EEPROM memory arrays to

thus provide a programmable EEPROM array with more reasonable current requirement, or else to program a larger EEPROM array with the same current source.

(2) With regard to claims 14-18, claims 10,11, and 13-15 of said copending application disclose a computer system with (A) central processing means (a CPU); (B) means (structure) for providing storage of data comprising (i) a side-wall memory array including a plurality of side-wall memory transistors and sets of bitlines, each side-wall memory transistor having a side-wall portion; (iii) a plurality of transferring means (switching circuits) for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array; and (iv) enabling means (logic circuitry) for enabling the plurality of transferring means (switching circuits) in a selected sequential order, wherein each of the side-wall memory transistors comprises: a gate electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer; a channel region formed below the gate electrode; a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units formed on the both sides of the gate electrode and having a function of retaining charges, and wherein the side-wall memory transistors are in sets and wherein selected transferring means (switching circuit) of the plurality of transferring means (switching circuits) is connected to a selected set of the sets of bitlines, and said selected transferring means (switching circuit) of the plurality of transferring means (switching circuits) is enabled to transfer a first voltage to the selected set of the sets of bitlines, the selected set being coupled to a

set of the sets of side-wall memory transistors to be programmed, until the set of side-wall memory transistors to be programmed has been programmed and the enabling means (logic circuitry) comprises a state machine, the state machine enabling each of the plurality of transferring means (switching circuits) such that the voltage is applied individually to the sets of bitlines until each set of the sets of bitlines has been programmed, and (C) a system bus means for transferring data and addresses between the central processing means and the means (structure) for providing storage of data. Claims 10,11, and 13-15 of said copending application do not disclose a charge pump for providing a voltage to accumulate negative charges in each memory transistor during a programming operation, or that the plurality of means for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array comprise four switching circuits, each switching circuit coupled to a corresponding set of four bitlines.

However, Larsen et al. discloses a computer system with a charge pump 30 for providing a voltage to accumulate negative charges in memory transistors during a programming operation and a plurality of means (switching circuits 44,45,46, and 47) for transferring the voltage to selected sets of a sets of bitlines of a memory array comprising four (44,45,46, and 47) switching circuits coupled to a corresponding set of four bitlines (seen without part # in figure 4, note column 8 line 11). Note figures 2-4, column 7 lines 7-40, and column 8 lines 4-17 of Larsen et al. Therefore, it would have been obvious to a person having skill in the art to augment claims 1-6 and 8 of said

copending application's computer system with the charge pump for providing a voltage to accumulate negative charges in each memory transistor during a programming operation and a plurality of means for transferring the voltage to selected sets of a sets of bitlines of a memory array comprising four switching circuits coupled to a corresponding set of four bitlines such as taught by Larsen et al. in order to reduce the amount of current used in programming flash EEPROM memory arrays to thus provide a programmable EEPROM array with more reasonable current.

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 8-11 and 19-21 are rejected under 35 U.S.C. 102(e) as being anticipated by KAMEI ET AL. (2003/0164517).

A. With regard to claims 8-10 Kamei et al. discloses a memory structure with (i) a memory array 200 including a plurality of memory transistors 100(i) and sets of bitlines BL(i), each memory transistor having a side-wall portion 109 and comprising a gate

electrode 104 formed on a semiconductor layer 102 with a gate insulating (gate oxide, no part #, see paragraph 0044) film formed on the semiconductor layer 102; a channel region formed below the gate electrode 104; a pair of diffusion regions 110(i) and 110(I+1) formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units 108A and 108B formed on the both sides of the gate electrode 104 and having a function of retaining charges; (ii) a charge pump (booster 430, see figure 8 and paragraphs 0093-0095) for providing a voltage to accumulate negative charges in the portion of each memory transistor during a programming operation; (iii) a plurality of switching circuits 452, 453, etc., see figure 11 for transferring the voltage to selected sets of the sets of bitlines BL(i) of the memory array 200; and (iv) logic circuitry – no part #s, seen just left of switches 452 etc. in figure 11 and described at paragraph 0104 for enabling the plurality of switching circuits in a selected sequential order, wherein the memory transistors 100(i) are in sets and wherein selected switching circuit of the plurality of switching circuits is connected to a selected set of the sets of bitlines BL(i), and said selected switching circuit of the plurality of switching circuits is enabled to transfer a first voltage to the selected set of the sets of bitlines BL(i), the selected set being coupled to a set of the sets of memory transistors 100(i) to be programmed, until the set of memory transistors 100(i) to be programmed has been programmed and the logic circuitry comprises a state machine, the state machine enabling each of the plurality of switching circuits such that the voltage is applied individually to the sets of bitlines BL(i) until each

set of the sets of bitlines BL(i) has been programmed. Note figures 1,9-11 and paragraphs 0036-0050 and 0093-0095 of Kamei et al.

B. With regard to claims 19-21 Kamei et al. discloses a structure for providing storage of data with (i) a memory array 200 including a plurality of memory transistors 100(i) and sets of bitlines BL(i), each memory transistor having a side-wall portion 109 and comprising a gate electrode 104 formed on a semiconductor layer 102 with a gate insulating (gate oxide, no part #, see paragraph 0044) film formed on the semiconductor layer 102; a channel region formed below the gate electrode 104; a pair of diffusion regions 110(i) and 110(I+1) formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units 108A and 108B formed on the both sides of the gate electrode 104 and having a function of retaining charges; (ii) a charge pump (booster 430, see figure 8 and paragraphs 0093-0095) for providing a voltage to accumulate negative charges in the portion of each memory transistor during a programming operation; (iii) a plurality of transferring means (switching circuits 452, 453, etc., see figure 11) for transferring the voltage to selected sets of the sets of bitlines BL(i) of the memory array 200; and (iv) enabling means (logic circuitry – no part #s, seen just left of switches 452 etc. in figure 11 and described at paragraph 0104) for enabling the plurality of transferring means (switching circuits) in a selected sequential order, wherein the memory transistors 100(i) are in sets and wherein selected transferring means (switching circuit) of the plurality of transferring means (switching circuits) is connected to a selected set of the sets of

bitlines BL(i), and said selected transferring means (switching circuit) of the plurality of transferring means (switching circuits) is enabled to transfer a first voltage to the selected set of the sets of bitlines BL(i), the selected set being coupled to a set of the sets of memory transistors 100(i) to be programmed, until the set of memory transistors 100(i) to be programmed has been programmed and the enabling means (logic circuitry) comprises a state machine, the state machine enabling each of the plurality of transferring means (switching circuits) such that the voltage is applied individually to the sets of bitlines BL(i) until each set of the sets of bitlines BL(i) has been programmed.

Note figures 1 and 9-11 and paragraphs 0036-0050 and 0093-0095 of Kamei et al.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over LARSEN ET AL. (5,537,350) in view of SAKAGAMI ET AL. (5,838,041).

(1) With regard to claims 1-7 Larsen et al. discloses a computer system with (A) a CPU 11 (central processor unit); (B) a memory arrangement comprising (i) a memory array including a plurality of memory transistors 28 and sets of bitlines (seen without

part # in figure 4, note column 8 line 11); (ii) a charge pump 22 for providing a voltage to accumulate negative charges in the portion of each memory transistor during a programming operation; (iii) a plurality of switching circuits 44,45,46, and 47 for transferring the voltage to selected sets of the sets of bitlines of the memory array; and (iv) logic circuitry 42 for enabling the plurality of switching circuits 44,45,46, and 47 in a selected sequential order, wherein the memory transistors 28 are in sets and wherein (one selected circuit out of the plurality of switching circuits 44,45,46, and 47 is connected to a selected set of the sets of bitlines, and said selected switching circuit of the plurality of switching circuits 44,45,46, and 47 is enabled to transfer a first voltage to the selected set of the sets of bitlines, the selected set being coupled to a set of the sets of memory transistors 28 to be programmed, until the set of memory transistors 28 to be programmed has been programmed and the logic circuitry 42 comprises a state machine (note figure 4 and column 8 lines 18-25, also see claim 2), the state machine enabling each of the plurality of switching circuits 44,45,46, and 47 such that the voltage is applied individually to the sets of bitlines until each set of the sets of bitlines has been programmed, the plurality of switching circuits 44,45,46, and 47 for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array comprise four (44,45,46, and 47) switching circuits 44,45,46, and 47, a switching circuit is coupled to a corresponding set of four bitlines; a bit line select circuit (seen without part # in figure 4, note column 8 line 11). coupled to the switching circuit to select bitlines of a set to connect to receive the voltage such that the selected bitlines are programmed; and

(C) a system bus 12 for transferring data and addresses between the CPU 11 and the memory arrangement. Note figures 1-4, column 7 lines 7-40, and column 8 lines 4-25 of Larsen et al. Larsen et al. does not disclose that each memory transistor has a side-wall portion and comprises a gate electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer; a channel region formed below the gate electrode; a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units formed on the both sides of the gate electrode and having a function of retaining charges.

However, Sakagami et al. discloses a computer system with memory transistors each having a side-wall portion 19 and comprising a gate electrode 13 formed on a semiconductor layer 1 with a gate insulating film 11 formed on the semiconductor layer 1; a channel region (no part #, it is the part of layer 1 seen directly below gate insulating film 11) formed below the gate electrode; a pair of diffusion regions 20,21 formed on the both sides of the channel region and having a conductive type opposite to that of the channel region, and a pair of memory functional units (charge trapping layers 17) formed on the both sides of the gate electrode 13 and having a function of retaining charges (regarding the memory function and the retaining charge function, note specifically column 4 lines 21 and 22). Note figures 2, 7, 8a, 8b, 15, column 4 lines 6-34, column 6 lines 48-66, and column 7 lines

1-17 of Sakagami et al. Therefore, it would have been obvious to a person having skill in the art to replace the memory transistors of Larsen et al.'s computer system with the memory transistors having side-wall portions and comprising a gate electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer; a channel region formed below the gate electrode; a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units formed on the both sides of the gate electrode and having a function of retaining charges such as taught by Sakagami et al. in order to allow the write cycle to reference drain 21 or source 20 and memory functional unit 18 during write operations to thus provide better more efficient write operation.

(2) With regard to claims 8-13 Larsen et al. discloses a memory structure with (i) a memory array including a plurality of memory transistors 28 and sets of bitlines (seen without part # in figure 4, note column 8 line 11); (ii) a charge pump 22 for providing a voltage to accumulate negative charges in the portion of each memory transistor during a programming operation; (iii) a plurality of switching circuits 44,45,46, and 47 for transferring the voltage to selected sets of the sets of bitlines of the memory array; and (iv) logic circuitry 42 for enabling the plurality of switching circuits 44,45,46, and 47 in a selected sequential order, wherein the memory transistors 28 are in sets and wherein (one selected circuit out of the plurality of switching circuits 44,45,46, and 47 is connected to a selected set of the sets of bitlines, and said selected switching circuit of

the plurality of switching circuits 44,45,46, and 47 is enabled to transfer a first voltage to the selected set of the sets of bitlines, the selected set being coupled to a set of the sets of memory transistors 28 to be programmed, until the set of memory transistors 28 to be programmed has been programmed and the logic circuitry 42 comprises a state machine (note figure 4 and column 8 lines 18-25, also see claim 2), the state machine enabling each of the plurality of switching circuits 44,45,46, and 47 such that the voltage is applied individually to the sets of bitlines until each set of the sets of bitlines has been programmed, the plurality of switching circuits 44,45,46, and 47 for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array comprise four (44,45,46, and 47) switching circuits 44,45,46, and 47, a switching circuit is coupled to a corresponding set of four bitlines; and further comprising a bit line select circuit (seen without part # in figure 4, note column 8 line 11). coupled to the switching circuit to select bitlines of a set to connect to receive the voltage such that the selected bitlines are programmed. Note figures 1-4, column 7 lines 7-40, and column 8 lines 4-25 of Larsen et al. Larsen et al. does not disclose that each memory transistor has a side-wall portion and comprises a gate electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer; a channel region formed below the gate electrode; a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units formed on the both sides of the gate electrode and having a function of retaining charges.

However, Sakagami et al. discloses a memory structure with memory transistors each having a side-wall portion 19 and comprising a gate electrode 13 formed on a semiconductor layer 1 with a gate insulating film 11 formed on the semiconductor layer 1, a channel region (no part #, it is the part of layer 1 seen directly below gate insulating film 11) formed below the gate electrode; a pair of diffusion regions 20,21 formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units (charge trapping layers 17) formed on the both sides of the gate electrode 13 and having a function of retaining charges (regarding the memory function and the retaining charge function, note specifically column 4 lines 21 and 22). Note figures 2, 7, 8a, 8b, 15, column 4 lines 6-34, column 6 lines 48-66, and column 7 lines 1-17 of Sakagami et al. Therefore, it would have been obvious to a person having skill in the art to replace the memory transistors of Larsen et al.'s memory structure with the memory transistors having side-wall portions and comprising a gate electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer; a channel region formed below the gate electrode; a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units formed on the both sides of the gate electrode and having a function of retaining charges such as taught by Sakagami et al. in order to allow the write cycle to reference drain 21 or source 20 and memory

functional unit 18 during write operations to thus provide better more efficient write operation.

(3) With regard to claims 14-18 Larsen et al. discloses a computer system with (A) central processing means (CPU 11); (B) means (structure) for providing storage of data comprising (i) a memory array including a plurality of memory transistors 28 and sets of bitlines (seen without part # in figure 4, note column 8 line 11); (ii) a charge pump 22 for providing a voltage to accumulate negative charges in the portion of each memory transistor during a programming operation; (iii) a plurality of transferring means (switching circuits 44,45,46, and 47) for transferring the voltage to selected sets of the sets of bitlines of the memory array; and (iv) enabling means (logic circuitry 42) for enabling the plurality of transferring means (switching circuits 44,45,46, and 47) in a selected sequential order, wherein the memory transistors 28 are in sets and wherein selected transferring means (one selected circuit out of 44,45,46, and 47) of the plurality of transferring means (switching circuits 44,45,46, and 47) is connected to a selected set of the sets of bitlines, and said selected transferring means (switching circuit) of the plurality of transferring means (switching circuits 44,45,46, and 47) is enabled to transfer a first voltage to the selected set of the sets of bitlines, the selected set being coupled to a set of the sets of memory transistors 28 to be programmed, until the set of memory transistors 28 to be programmed

has been programmed and the enabling means (logic circuitry 42) comprises a state machine (note figure 4 and column 8 lines 18-25, also see claim 2), the state machine enabling each of the plurality of transferring means (switching circuits 44,45,46, and 47) such that the voltage is applied individually to the sets of bitlines until each set of the sets of bitlines has been programmed, the plurality of transferring means (switching circuits 44,45,46, and 47) for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array comprise four (44,45,46, and 47) switching circuits 44,45,46, and 47, a switching circuit is coupled to a corresponding set of four bitlines; and (C) a system bus 12 means for transferring data and addresses between the central processing means and the means (structure) for providing storage of data. Note figures 1-4, column 7 lines 7-40, and column 8 lines 4-25 of Larsen et al. Larsen et al. does not disclose that each memory transistor has a side-wall portion and comprises a gate electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer; a channel region formed below the gate electrode; a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units formed on the both sides of the gate electrode and having a function of retaining charges.

However, Sakagami et al. discloses a computer system with memory transistors each having a side-wall portion 19 and comprising a gate electrode 13 formed on a

semiconductor layer 1 with a gate insulating film 11 formed on the semiconductor layer 1; a channel region (no part #, it is the part of layer 1 seen directly below gate insulating film 11) formed below the gate electrode; a pair of diffusion regions 20,21 formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units (charge trapping layers 17) formed on the both sides of the gate electrode 13 and having a function of retaining charges (regarding the memory function and the retaining charge function, note specifically column 4 lines 21 and 22). Note figures 2, 7, 8a, 8b, 15, column 4 lines 6-34, column 6 lines 48-66, and column 7 lines 1-17 of Sakagami et al. Therefore, it would have been obvious to a person having skill in the art to replace the memory transistors of Larsen et al.'s computer system with the memory transistors having side-wall portions and comprising a gate electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer; a channel region formed below the gate electrode; a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units formed on the both sides of the gate electrode and having a function of retaining charges such as taught by Sakagami et al. in order to allow the write cycle to reference drain 21 or source 20 and memory functional unit 18 during write operations to thus provide better more efficient write operation.

(4) With regard to claims 19-23 Larsen et al. discloses a structure for providing storage of data with (i) a memory array including a plurality of memory transistors 28 and sets of bitlines (seen without part # in figure 4, note column 8 line 11); (ii) a charge pump 22 for providing a voltage to accumulate negative charges in the portion of each memory transistor during a programming operation; (iii) a plurality of transferring means (switching circuits 44,45,46, and 47) for transferring the voltage to selected sets of the sets of bitlines of the memory array; and (iv) enabling means (logic circuitry 42) for enabling the plurality of transferring means (switching circuits 44,45,46, and 47) in a selected sequential order, wherein the memory transistors 28 are in sets and wherein selected transferring means (one selected circuit out of 44,45,46, and 47) of the plurality of transferring means (switching circuits 44,45,46, and 47) is connected to a selected set of the sets of bitlines, and said selected transferring means (switching circuit) of the plurality of transferring means (switching circuits 44,45,46, and 47) is enabled to transfer a first voltage to the selected set of the sets of bitlines, the selected set being coupled to a set of the sets of memory transistors 28 to be programmed, until the set of memory transistors 28 to be programmed has been programmed and the enabling means (logic circuitry 42) comprises a state machine (note figure 4 and column 8 lines 18-25, also see claim 2), the state machine enabling each of the plurality of transferring means (switching circuits 44,45,46, and 47) such that the voltage is applied individually to the sets of bitlines until each set of the sets of bitlines has been programmed, the plurality of transferring means (switching circuits 44,45,46, and 47) for transferring the

voltage to selected sets of the sets of bitlines of the side-wall memory array comprise four (44,45,46, and 47) switching circuits 44,45,46, and 47, a switching circuit is coupled to a corresponding set of four bitlines. Note figures 1-4, column 7 lines 7-40, and column 8 lines 4-25 of Larsen et al. Larsen et al. does not disclose that each memory transistor has a side-wall portion and comprises a gate electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer; a channel region formed below the gate electrode; a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units formed on the both sides of the gate electrode and having a function of retaining charges.

However, Sakagami et al. discloses a structure for providing storage of data with memory transistors each having a side-wall portion 19 and comprising a gate electrode 13 formed on a semiconductor layer 1 with a gate insulating film 11 formed on the semiconductor layer 1; a channel region (no part #, it is the part of layer 1 seen directly below gate insulating film 11) formed below the gate electrode; a pair of diffusion regions 20,21 formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units (charge trapping layers 17) formed on the both sides of the gate electrode 13 and having a function of retaining charges (regarding the memory function and the retaining charge function, note specifically column 4 lines 21 and 22). Note figures 2, 7, 8a, 8b, 15, column 4 lines 6-34, column 6 lines 48-66, and column 7 lines 1-17 of Sakagami et

al. Therefore, it would have been obvious to a person having skill in the art to replace the memory transistors of Larsen et al.'s structure for providing storage of data with the memory transistors having side-wall portions and comprising a gate electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer; a channel region formed below the gate electrode; a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units formed on the both sides of the gate electrode and having a function of retaining charges such as taught by Sakagami et al. in order to allow the write cycle to reference drain 21 or source 20 and memory functional unit 18 during write operations to thus provide better more efficient write operation.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thomas L. Dickey
Patent Examiner
Art Unit 2826
08/05

EVAN PERT
PRIMARY EXAMINER